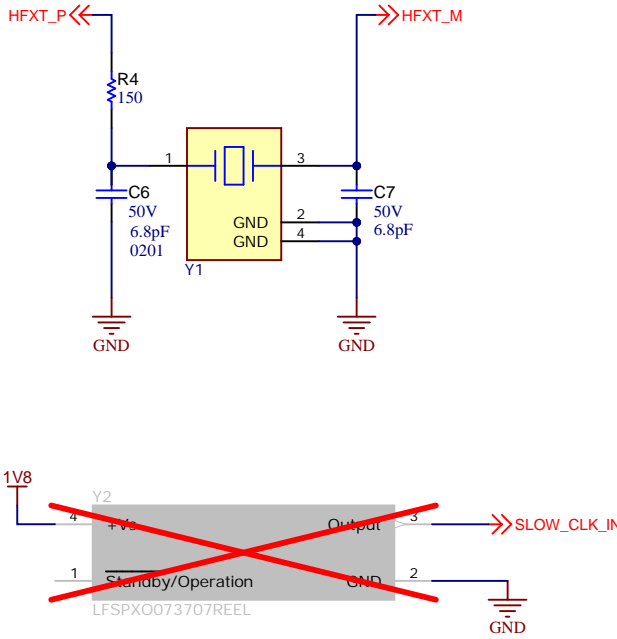


Clock

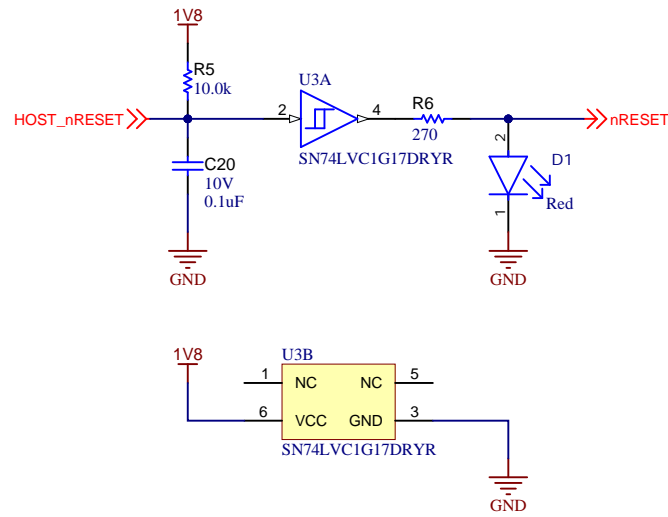


Orderable: N/A	Designed for: Public Release	Mod. Date: 2/2/2024	
TID #: N/A	Project Title: TD-CC3351		
Number: MCU127	Rev: A	Sheet Title:	
SVN Ref: acc4e8a24d3bc41063b3858555f9bdc651	Antenna	Sheet: 1 of 3	
Drawn by: Jessica M. Torres	File: MCU127-TD-CC3351_EngineArea_SchDoc	Size: B	
Engineer: Jessica M. Torres	Contact: http://www.ti.com/support		http://www.ti.com © Texas Instruments 2024

Level Shifters

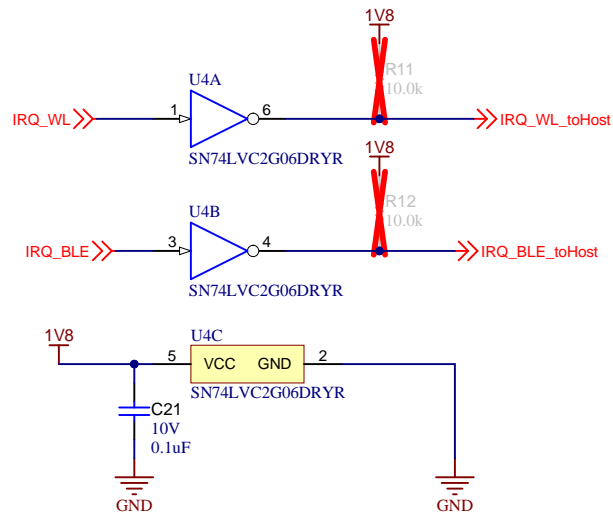
The Level Shifter (U3) is placed to make sure the device receives a 1.8V for the nRESET (Active Low) signal. As such the device is protected from legacy 3.3V adapter as the PCIE Specification mentions.

The RC circuit (R5 and C20) is placed to apply a recommended 1ms delay to the nRESET signal.

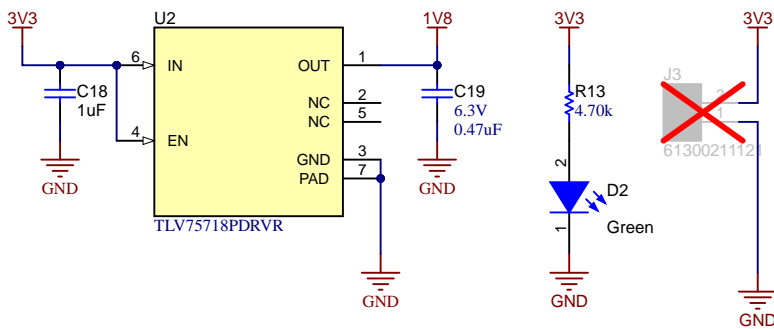


The "Dual Inverter Buffer with Open-Drain Output" (U4) allows the device to output the interrupt lines as Active Low to conform to the PCIE M.2 Specification.

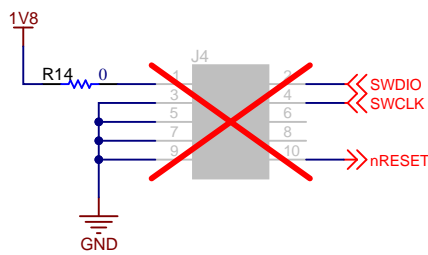
The R11 and R12 resistor are not populated, the pads are provided in the off case the host platform does not have these lines pulled up as the PCIE M.2 specification metions.



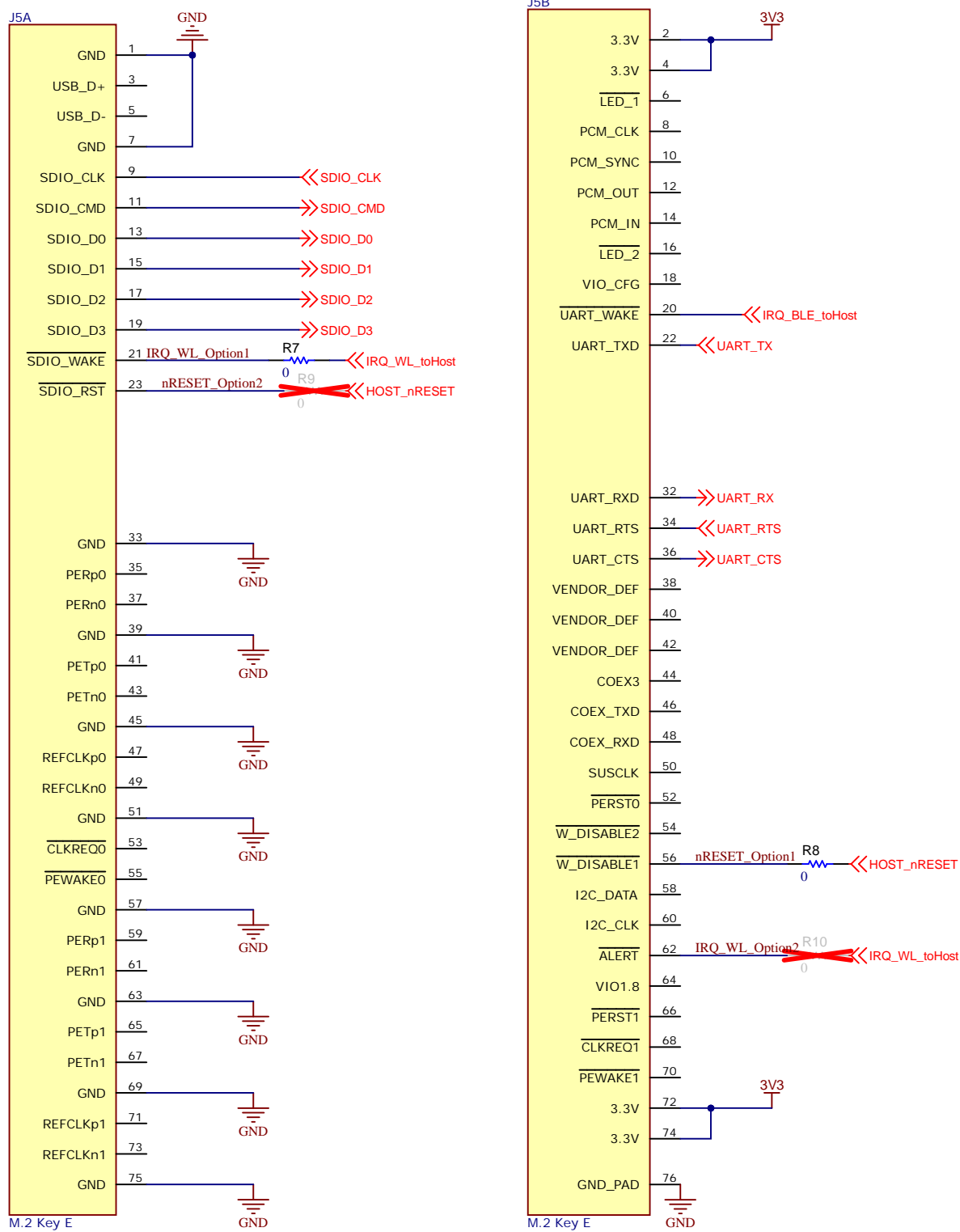
Power



XDS110 Connector



M.2 Type Key E Connector



The M2-CC3301 Gold finger Edge connector (J5A and J5B) follows the PCIE M.2 form factor Type 2230 Key E, as such the board can be compatible with any host that has a 75-position host interface connector for this type. Refer to the User Guide (Lit# SWAU131) for more information on the pin out.

Note only resistors R7 and R8 will be populated, they can be swapped to R9 and R10 positions for adapting to the expected pinout a host platform expects.

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Orderable: M2-CC3301	Designed for: Public Release	Mod. Date: 2/2/2024
TID #: N/A	Project Title: M2-CC3351	
Number: MCU127	Rev: A	Sheet Title:
S/N Rev: acc4a8a24df3bcdf11063b	Rev: A	Sheet 2 of 3
Drawn By: Jessica M. Torres	File: MCU127_M2-CC3351_M2-Connector_SchDoc	Size: B
Engineer: Jessica M. Torres	Contact: http://www.ti.com/support	http://www.ti.com



